

# Exhibit 6

M386A8K40BM1

M386A8K40BM2

# 288pin Load Reduced DIMM based on 8Gb B-die

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78FBGA with Lead-Free & Halogen-Free  
(RoHS compliant)

## datasheet

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Load Reduced DIMM

datasheet

DDR4 SDRAM

## Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>	<u>Editor</u>
1.0	- First SPEC Release	Apr. 2015	-	J.Y.Lee
1.1	- Change of IDD value on page 25	2nd Feb. 2016	-	J.Y.Lee
	- Change of 8.1 Timing & Capacitance values (tACT) on page 9			
	- Change of Physical Dimensions (Module Thickness) on page 38			
1.2	- Addition of DDR4-2666	7th Apr. 2016	-	J.Y.Lee
1.21	- Correction of typo.	18th Apr. 2016	-	S.H.Kim
1.3	- Addition of IDD value (2666Mbps) on page 25	17th Nov. 2016	-	J.Y.Lee
1.4	- Update Physical dimension.	8th Jun, 2017	Final	J.Y.Bae
	1. Add PCB hole.			
	2. Update Module height information.			
	- Update Absolute Maximum Ratings.			
	- Update Input/Output Capacitance.			

## Table Of Contents

### **288pin Load Reduced DIMM based on 8Gb B-die**

1. DDR4 Load Reduced DIMM Ordering Information .....	4
2. Key Features .....	4
3. Address Configuration .....	4
4. Load Reduced DIMM Pin Configurations (Front side/Back side) .....	5
5. Pin Description .....	6
6. ON DIMM Thermal Sensor .....	6
7. Input/Output Functional Description .....	7
8. Registering Clock Driver Specification .....	9
8.1 Timing & Capacitance Values .....	9
8.2 Clock Driver Characteristics .....	9
9. Function Block Diagram: .....	10
9.1 64GB, 8Gx72 Module (Populated as 4 ranks of x4 DDR4 SDRAMs) .....	10
10. Absolute Maximum Ratings .....	13
10.1 Absolute Maximum DC Ratings .....	13
11. AC & DC Operating Conditions .....	13
11.1 Recommended DC Operating Conditions .....	13
12. AC & DC Input Measurement Levels .....	14
12.1 AC & DC Logic Input Levels for Single-Ended Signals .....	14
12.2 AC and DC Input Measurement Levels: VREF Tolerances .....	14
12.3 AC and DC Logic Input Levels for Differential Signals .....	15
12.3.1. Differential Signals Definition .....	15
12.3.2. Differential Swing Requirements for Clock (CK_t - CK_c) .....	15
12.3.3. Single-ended Requirements for Differential Signals .....	16
12.4 Slew Rate Definitions .....	17
12.4.1. Slew Rate Definitions for Differential Input Signals (CK) .....	17
12.5 Differential Input Cross Point Voltage .....	18
12.6 Single-ended AC & DC Output Levels .....	19
12.7 Differential AC & DC Output Levels .....	19
12.8 Single-ended Output Slew Rate .....	19
12.9 Differential Output Slew Rate .....	20
12.10 Single-ended AC & DC Output Levels of Connectivity Test Mode .....	21
12.11 Test Load for Connectivity Test Mode Timing .....	21
13. DIMM IDD Specification Definition .....	22
14. IDD SPEC Table .....	25
15. Input/Output Capacitance .....	27
16. Electrical Characteristics and AC Timing .....	28
16.1 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin .....	28
16.2 Speed Bin Table Note .....	33
17. Timing Parameters by Speed Grade .....	34
18. Physical Dimensions .....	40
18.1 4Gbx4(DDP) based 8Gx72 Module (4 Ranks) - M386A8K40BM1/M386A8K40BM2 .....	40
18.1.1. x72 DIMM, populated as Quad physical ranks of x4 DDR4 SDRAMs .....	40
18.1.2. Heat Spreader Design Guide .....	41

## 1. DDR4 Load Reduced DIMM Ordering Information

Part Number <sup>2</sup>	Density	Organization	Component Composition <sup>1</sup>	Number of Rank	Height
M386A8K40BM1-CPB/RC	64GB	8Gx72	DDP 4Gx4(K4AAG045WB-MC##)*36	4	31.25mm
M386A8K40BM2-CTD	64GB	8Gx72	DDP 4Gx4(K4AAG045WB-MC##)*36	4	31.25mm

**NOTE :**

1. "##" - PB/RC/TD

2. PB(2133Mbps 15-15-15)/RC(2400Mbps 17-17-17)/TD(2666Mbps 19-19-19)

- DDR4-2666(19-19-19) is backward compatible to DDR4-2400(17-17-17)

## 2. Key Features

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	
tCK(min)	1.25	1.071	0.938	0.833	0.75	ns
CAS Latency	11	13	15	17	19	nCK
tRCD(min)	13.75	13.92	14.06	14.16	14.25	ns
tRP(min)	13.75	13.92	14.06	14.16	14.25	ns
tRAS(min)	35	34	33	32	32	ns
tRC(min)	48.75	47.92	47.06	46.16	46.25	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V<sub>DDQ</sub> = 1.2V ± 0.06V
- 800 MHz f<sub>CK</sub> for 1600Mb/sec/pin, 933 MHz f<sub>CK</sub> for 1866Mb/sec/pin, 1067MHz f<sub>CK</sub> for 2133Mb/sec/pin, 1200MHz f<sub>CK</sub> for 2400Mb/sec/pin, 1333MHz f<sub>CK</sub> for 2666Mb/sec/pin
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 10,11,12,13,14,15,16,17,18,19,20
- Programmable Additive Latency (Posted CAS): 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866), 11,14 (DDR4-2133), 12,16 (DDR4-2400) and 14,18 (DDR4-2666)
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T<sub>CASE</sub> 85°C, 3.9us at 85°C < T<sub>CASE</sub> ≤ 95°C
- Asynchronous Reset

## 3. Address Configuration

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
4Gx4(16Gb DDP) based Module	A0-A16	A0-A9	BG0-BG1	BA0-BA1	A10/AP

## 4. Load Reduced DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V <sup>3</sup> ,NC	145	12V <sup>3</sup> ,NC	40	TDQS12_t, DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	TDQS12_c, DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	TDQS15_t, DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	TDQS15_c, DQS15_c	266	DQS6_c
7	TDQS9_t, DQS9_t	151	VSS	46	VSS	190	DQ27	84	S0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	TDQS9_c, DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	TDQS17_t, DQS17_t	195	VSS	89	S1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	TDQS17_c, DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	NC,C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n,NC	237	NC,CS3_c,C1	132	TDQS16_t, DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	TDQS16_c, DQS16_c	277	DQS7_c
18	TDQS10_t, DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	TDQS10_c, DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	TDQS13_t, DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	TDQS13_c, DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP <sup>4</sup>
29	TDQS11_t, DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	TDQS11_c, DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	TDQS14_t, DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	TDQS14_c, DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

### NOTE:

1. VPP is 2.5V DC
2. Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE\_n for NVDIMMs.
3. Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
4. The 5th VPP is required on all modules. DIMMs.

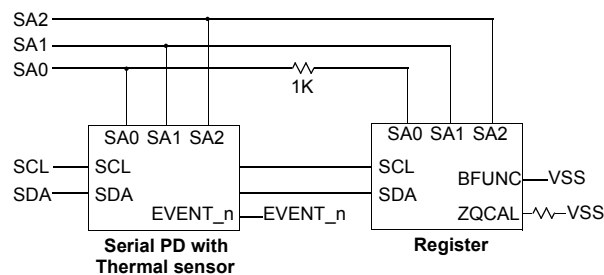
## 5. Pin Description

Pin Name	Description	Pin Name	Description
A0–A17 <sup>1</sup>	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0–SA2	I2C slave address select for SPD/TS and register
RAS_n <sup>2</sup>	Register row address strobe input	PAR	Register parity input
CAS_n <sup>3</sup>	Register column address strobe input	VDD	SDRAM core power supply
WE_n <sup>4</sup>	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input for activate input	ALERT_n	Register ALERT_n output
DQ0–DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0–CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RFU	Reserved for future use
CK0_t, CK1_t	Register clock input (positive line of differential pair)		
CK0_c, CK1_c	Register clocks input (negative line of differential pair)		

### NOTE :

1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS\_n is a multiplexed function with A16.
3. CAS\_n is a multiplexed function with A15.
4. WE\_n is a multiplexed function with A14.

## 6. ON DIMM Thermal Sensor



NOTE : 1. All Samsung RDIMM support Thermal sensor on DIMM

[ Table 1 ] Temperature Sensor Characteristics

Grade	Range	Temperature Sensor Accuracy			Units	NOTE
		Min.	Typ.	Max.		
B	75 < Ta < 95	-	+/- 0.5	+/- 1.0	°C	-
	40 < Ta < 125	-	+/- 1.0	+/- 2.0		-
	-20 < Ta < 125	-	+/- 2.0	+/- 3.0		-
Resolution		0.25			°C /LSB	-

## 7. Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1	Input	Chip ID : Chip ID is only used for 3DS for 2and4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components only BG0 is valid.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.



## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

Symbol	Type	Function
PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Output	ALERT: It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system. In case of not connected as Signal, ALERT_n Pin must be connected to VDD on DIMM.
SA0-SA1	Input	Device address for the SPD.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
NC		No Connect: No on DIMM electrical connection is present.
VDD <sup>1</sup>	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VTT <sup>2</sup>	Supply	Power Supply: 0.6 V
VPP	Supply	DRAM Activating Power Supply: 2.5V ( 2.375V min , 2.75V max)
VREFCA	Supply	Reference voltage for CA
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD 2.5V ± 10%.

**NOTE :**

1. For PC4, VDD is 1.2 V. For PC4L VDD is TBD.
2. For PC4, VTT is 0.6 V. For PC4L VTT is TBD.

## 8. Registering Clock Driver Specification

### 8.1 Timing & Capacitance Values

Symbol	Parameter	Conditions	DDR4-1600/1866/2133		DDR4-2400/2666		Units	Notes
			Min	Max	Min	Max		
f <sub>clock</sub>	Input Clock Frequency	application frequency	625	1080	625	1350	MHz	
t <sub>CH</sub> /t <sub>CL</sub>	Pulse duration, CK_t, CK_c HIGH or LOW		0.4	-	0.4	-	t <sub>CK</sub>	
t <sub>ACT</sub>	Inputs active time before DRST_n is taken HIGH	DCKE0/1 = LOW and DCS0/1_n = HIGH	16	-	16	-	t <sub>CK</sub>	
t <sub>PDM</sub>	Propagation delay, single-bit switching, CK_t/ CK_c to output	1.2V Operation	1	1.3	1	1.3	ns	
t <sub>DIS</sub>	output disable time	Rising edge of Yn_t to output float	0.5*t <sub>CK</sub> + t <sub>QSK1</sub> (min)	-	0.5*t <sub>CK</sub> + t <sub>QSK1</sub> (min)	-	ps	
t <sub>EN</sub>	output enable time	Output valid to rising edge of Yn_t	0.5*t <sub>CK</sub> - t <sub>QSK1</sub> (max)	-	0.5*t <sub>CK</sub> - t <sub>QSK1</sub> (max)	-	ps	
C <sub>I</sub>	Input capacitance, Data inputs	NOTE <sup>1,2</sup>	0.8	1.1	0.8	1.0	pF	
C <sub>CK</sub>	Input capacitance, CK_t, CK_c	NOTE <sup>1,2</sup>	0.8	1.1	0.8	1.0		
C <sub>IR</sub>	Input capacitance, DRST_n	V <sub>I</sub> =V <sub>DD</sub> or V <sub>SS</sub> ; V <sub>DD</sub> =1.2V	0.5	2.0	0.5	2.0		

**Note:**

1. This parameter does not include package capacitance

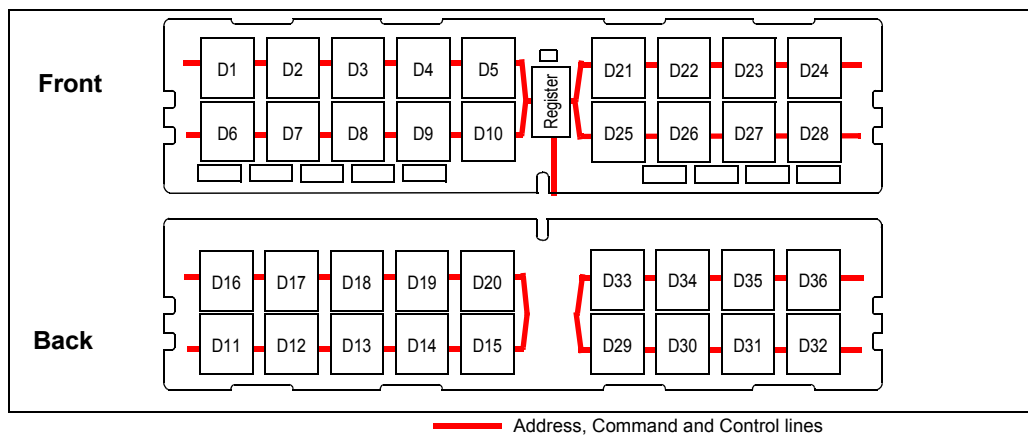
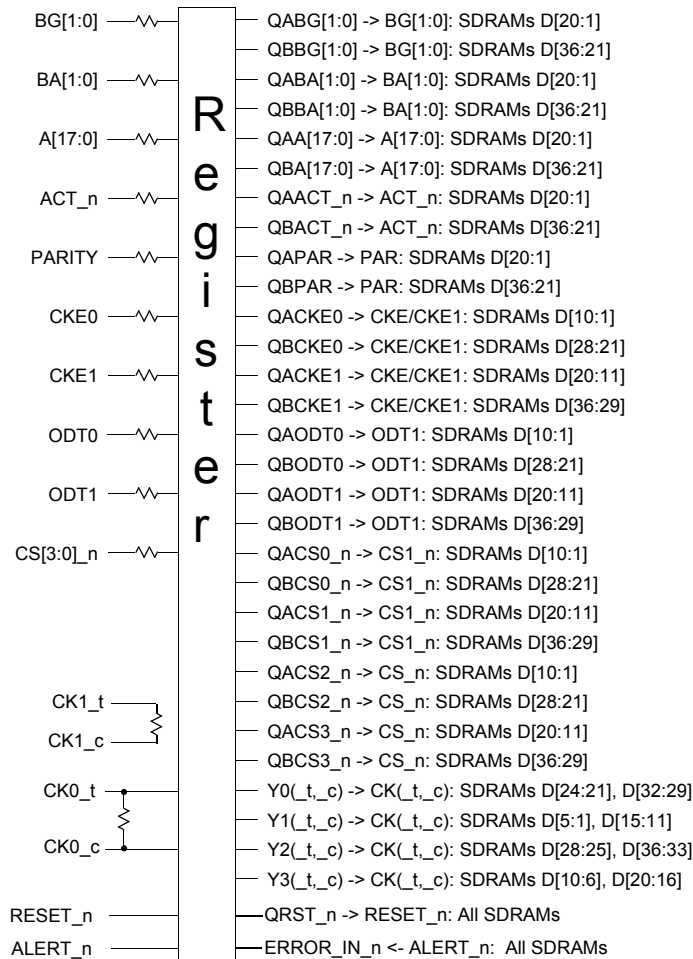
2. Data inputs are DCKE0/1, DODT0/1, DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT\_n, DC0..DC2, DPAR, DCS0/1\_n

### 8.2 Clock Driver Characteristics

Symbol	Parameter	Conditions	DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		Units	Notes
			Min	Max	Min	Max	Min	Max		
t <sub>jitter</sub> (cc)	Cycle-to-cycle period jitter	CK_t/CK_c stable	0	0.025 x t <sub>CK</sub>	0	0.025 x t <sub>CK</sub>	0	0.025 x t <sub>CK</sub>	ps	
t <sub>STAB</sub>	Stabilization time		-	5	-	5	-	5	us	
t <sub>CKsk</sub>	Clock Output skew		-	10	-	10	-	10	ps	
t <sub>jitter</sub> (per)	Yn Clock Period jitter		-0.025 * t <sub>CK</sub>	0.025 * t <sub>CK</sub>	-0.025 * t <sub>CK</sub>	0.025 * t <sub>CK</sub>	-0.025 * t <sub>CK</sub>	0.025 * t <sub>CK</sub>	ps	
t <sub>jitter</sub> (hper)	Half period jitter		-0.032 * t <sub>CK</sub>	0.032 * t <sub>CK</sub>	-0.032 * t <sub>CK</sub>	0.032 * t <sub>CK</sub>	-0.032 * t <sub>CK</sub>	0.032 * t <sub>CK</sub>	ps	
t <sub>Qsk1</sub>	Qn Output to clock tolerance		-0.125 * t <sub>CK</sub>	0.125 * t <sub>CK</sub>	-0.125 * t <sub>CK</sub>	0.125 * t <sub>CK</sub>	-0.1 * t <sub>CK</sub>	0.1 * t <sub>CK</sub>	ps	
t <sub>dynoff</sub>	Maximum re-driven dynamic clock off-set		-	50	-	45	-	45	ps	

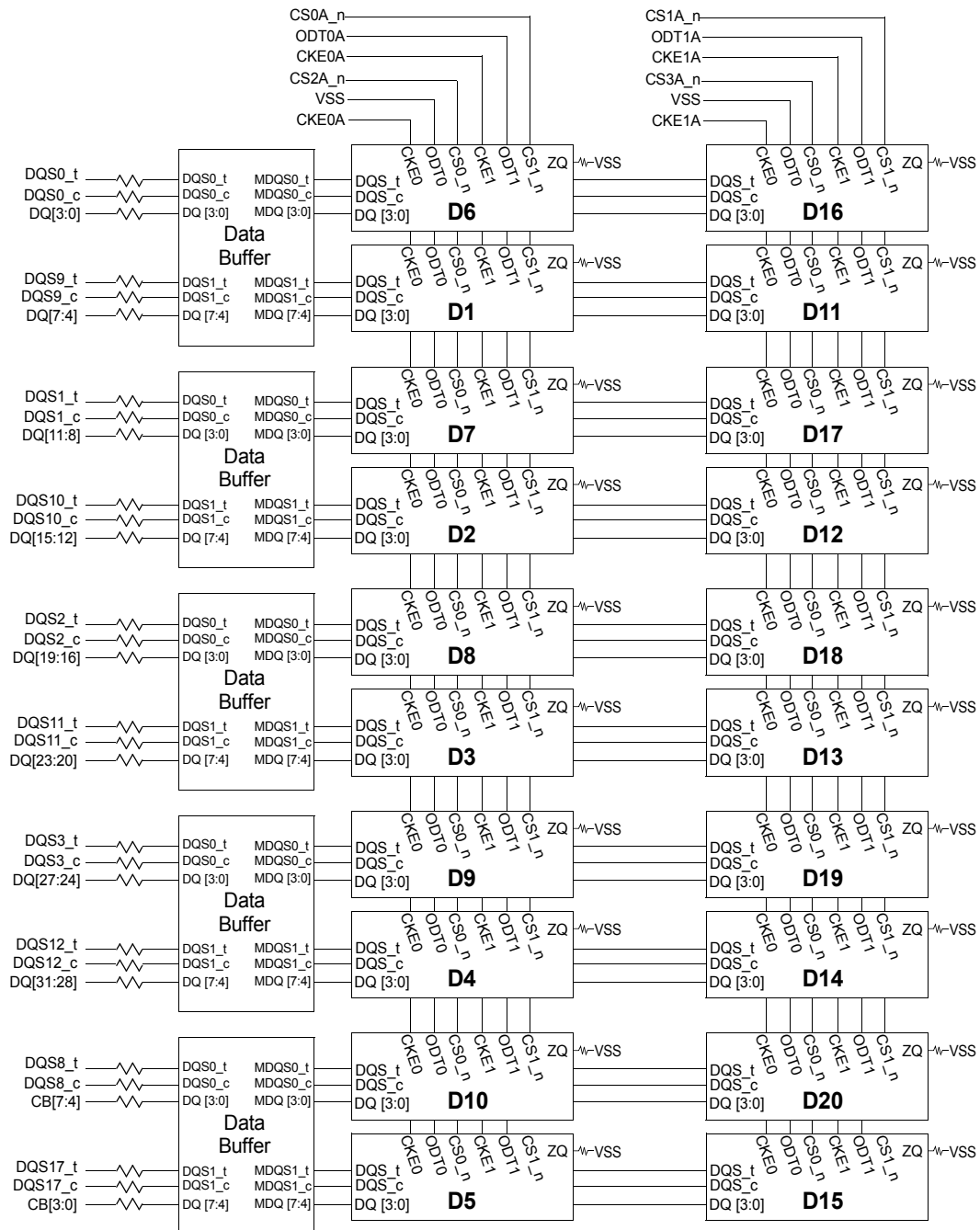
## 9. Function Block Diagram:

### 9.1 64GB, 8Gx72 Module (Populated as 4 ranks of x4 DDR4 SDRAMs)



#### NOTE :

1. CK0\_t, CK0\_c terminated with  $120\Omega \pm 5\%$  resistor.
2. CK1\_t, CK1\_c terminated with  $120\Omega \pm 5\%$  resistor but not used.
3. Unless otherwise noted resistors are  $22\Omega \pm 5\%$ .



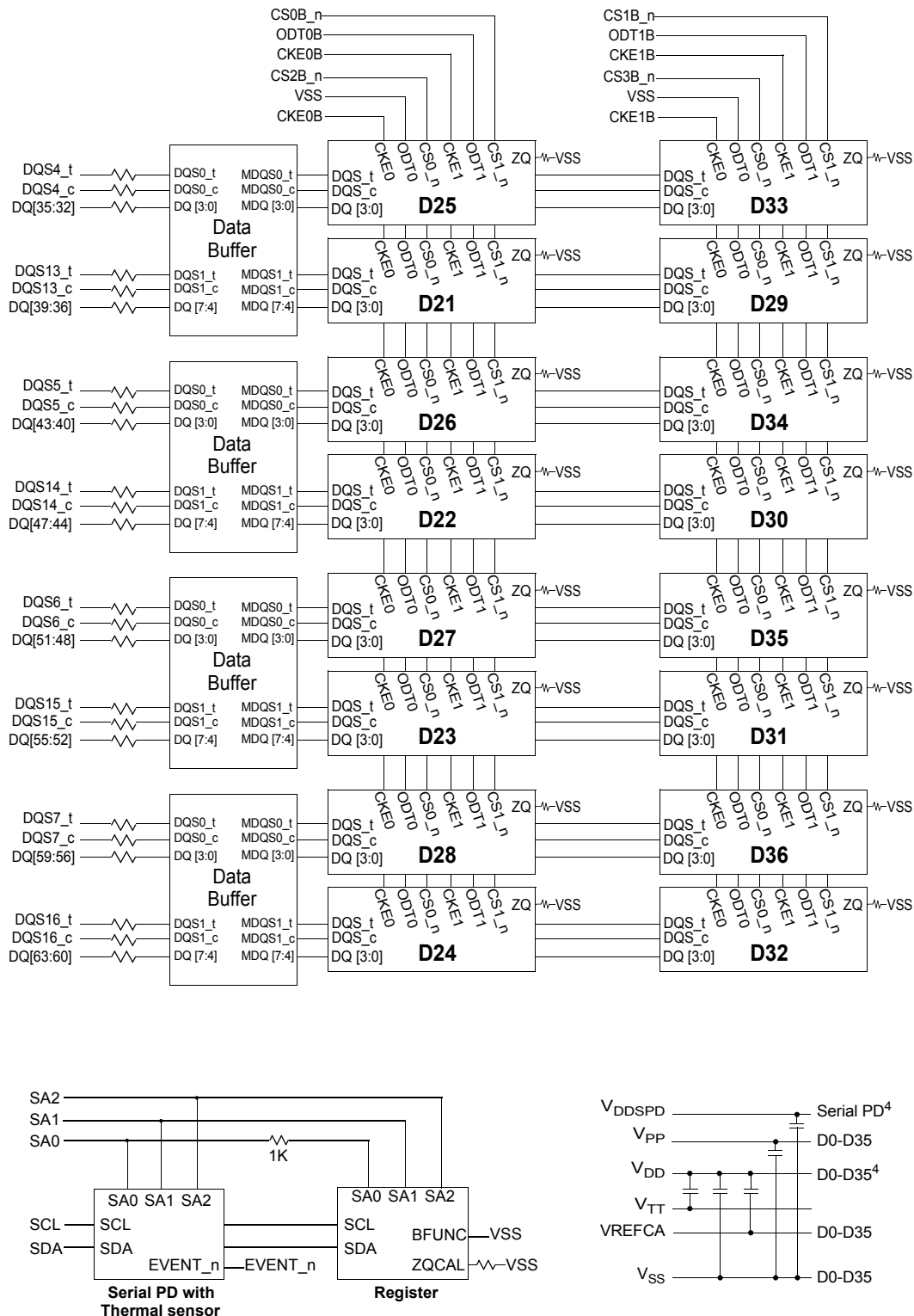
**NOTE :**

1. ZQ resistors are  $240\Omega \pm 1\%$ . For all other resistor values refer to the appropriate wiring diagram.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. TEN pin of SDRAMs is tied to VSS.

## Load Reduced DIMM

## datasheet

## DDR4 SDRAM



## NOTE :

1. ZQ resistors are  $240\Omega \pm 1\%$ . For all other resistor values refer to the appropriate wiring diagram.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. TEN pin of SDRAMs is tied to VSS.
4. VDDSPD is also applied to the register. VDD is also applied to the register and the data buffers.

## 10. Absolute Maximum Ratings

### 10.1 Absolute Maximum DC Ratings

[ Table 2 ] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin except VREFCA to Vss	-0.3 ~ 1.5	V	1,3
T <sub>STG</sub>	Storage Temperature	-55 to +100	°C	1,2

**NOTE:**

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ. When VDD and VDDQ are less than 500mV, VREFCA may be equal to or less than 300mV.
- VPP must be equal or greater than VDD/VDDQ at all times.

## 11. AC & DC Operating Conditions

### 11.1 Recommended DC Operating Conditions

[ Table 3 ] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

**NOTE:**

- Under all conditions V<sub>DDQ</sub> must be less than or equal to V<sub>DD</sub>.
- V<sub>DDQ</sub> tracks with V<sub>DD</sub>. AC parameters are measured with V<sub>DD</sub> and V<sub>DDQ</sub> tied together.
- DC bandwidth is limited to 20MHz.

## 12. AC & DC Input Measurement Levels

### 12.1 AC & DC Logic Input Levels for Single-Ended Signals

[ Table 4 ] Single-ended AC & DC Input Levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666		Unit	NOTE
		Min.	Max.	Min.	Max.		
$V_{IH.CA}(DC75)$	DC input logic high	$V_{REFCA} + 0.075$	$V_{DD}$	TBD	TBD	V	
$V_{IL.CA}(DC75)$	DC input logic low	$V_{SS}$	$V_{REFCA} - 0.075$	TBD	TBD	V	
$V_{IH.CA}(AC100)$	AC input logic high	$V_{REF} + 0.1$	Note 2	TBD	TBD	V	1
$V_{IL.CA}(AC100)$	AC input logic low	Note 2	$V_{REF} - 0.1$	TBD	TBD	V	1
$V_{REFCA}(DC)$	Reference Voltage for ADD, CMD inputs	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	TBD	TBD	V	2,3

**NOTE:**

1. See "Overshoot and Undershoot Specifications" on section.
2. The AC peak noise on  $V_{REFCA}$  may not allow  $V_{REFCA}$  to deviate from  $V_{REFCA}(DC)$  by more than  $\pm 1\% V_{DD}$  (for reference : approx.  $\pm 12mV$ )
3. For reference : approx.  $V_{DD}/2 \pm 12mV$

### 12.2 AC and DC Input Measurement Levels: $V_{REF}$ Tolerances.

The DC-tolerance limits and ac-noise limits for the reference voltages  $V_{REFCA}$  is illustrated in Figure 1. It shows a valid reference voltage  $V_{REF}(t)$  as a function of time. ( $V_{REF}$  stands for  $V_{REFCA}$ ).

$V_{REF}(DC)$  is the linear average of  $V_{REF}(t)$  over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore  $V_{REF}(t)$  may temporarily deviate from  $V_{REF}(DC)$  by no more than  $\pm 1\% V_{DD}$ .

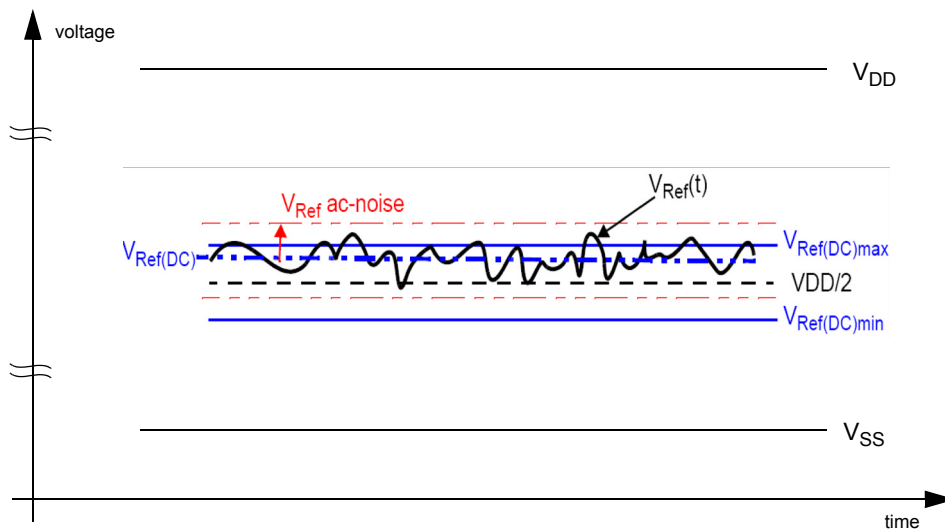


Figure 1. Illustration of  $V_{REF}(DC)$  tolerance and  $V_{REF}$  AC-noise limits

The voltage levels for setup and hold time measurements  $V_{IH}(AC)$ ,  $V_{IH}(DC)$ ,  $V_{IL}(AC)$  and  $V_{IL}(DC)$  are dependent on  $V_{REF}$ .

" $V_{REF}$ " shall be understood as  $V_{REF}(DC)$ , as defined in Figure 1.

This clarifies, that DC-variations of  $V_{REF}$  affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for  $V_{REF}(DC)$  deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with  $V_{REF}$  AC-noise. Timing and voltage effects due to AC-noise on  $V_{REF}$  up to the specified limit ( $\pm 1\%$  of  $V_{DD}$ ) are included in DRAM timings and their associated deratings.

## 12.3 AC and DC Logic Input Levels for Differential Signals

### 12.3.1 Differential Signals Definition

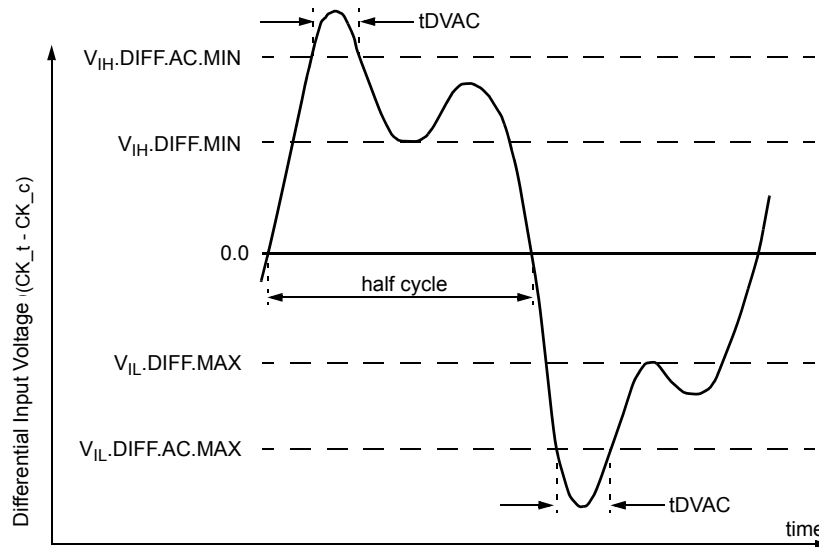


Figure 2. Definition of differential ac-swing and “time above ac-level”  $t_{DVAC}$

**NOTE:**

1. Differential signal rising edge from  $V_{IL,DIFF,MAX}$  to  $V_{IH,DIFF,MIN}$  must be monotonic slope.
2. Differential signal falling edge from  $V_{IH,DIFF,MIN}$  to  $V_{IL,DIFF,MAX}$  must be monotonic slope.

### 12.3.2 Differential Swing Requirements for Clock ( $CK_t - CK_c$ )

[ Table 5 ] Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600/1866/2133		DDR4 -2400/2666		unit	NOTE
		min	max	min	max		
$V_{IHdiff}$	differential input high	+0.150	NOTE 3	TBD	NOTE 3	V	1
$V_{ILdiff}$	differential input low	NOTE 3	-0.150	NOTE 3	TBD	V	1
$V_{IHdiff}(AC)$	differential input high ac	$2 \times (V_{IH}(AC) - V_{REF})$	NOTE 3	$2 \times (V_{IH}(AC) - V_{REF})$	NOTE 3	V	2
$V_{ILdiff}(AC)$	differential input low ac	NOTE 3	$2 \times (V_{IL}(AC) - V_{REF})$	NOTE 3	$2 \times (V_{IL}(AC) - V_{REF})$	V	2

**NOTE:**

1. Used to define a differential signal slew-rate.
2. for  $CK_t - CK_c$  use  $V_{IH,CA}/V_{IL,CA}(AC)$  of ADD/CMD and  $V_{REFCA}$ .
3. These values are not defined; however, the differential signals  $CK_t - CK_c$ , need to be within the respective limits ( $V_{IH,CA}(DC)$  max,  $V_{IL,CA}(DC)$  min) for single-ended signals as well as the limitations for overshoot and undershoot.

[ Table 6 ] Allowed Time Before Ringback ( $t_{DVAC}$ ) for  $CK_t - CK_c$

Slew Rate [V/ns]	$t_{DVAC}$ [ps] @ $ V_{IH/Ldiff}(AC)  = 200mV$	
	min	max
> 4.0	120	-
4.0	115	-
3.0	110	-
2.0	105	-
1.8	100	-
1.6	95	-
1.4	90	-
1.2	85	-
1.0	80	-
< 1.0	80	-



### 12.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK<sub>t</sub>, CK<sub>c</sub>) has also to comply with certain requirements for single-ended signals.

CK<sub>t</sub> and CK<sub>c</sub> have to approximately reach V<sub>SEH</sub>min / V<sub>SEL</sub>max (approximately equal to the ac-levels (V<sub>IH</sub>.CA(AC) / V<sub>IL</sub>.CA(AC)) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than V<sub>IH</sub>.CA(AC100)/V<sub>IL</sub>.CA(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK<sub>t</sub> and CK<sub>c</sub>

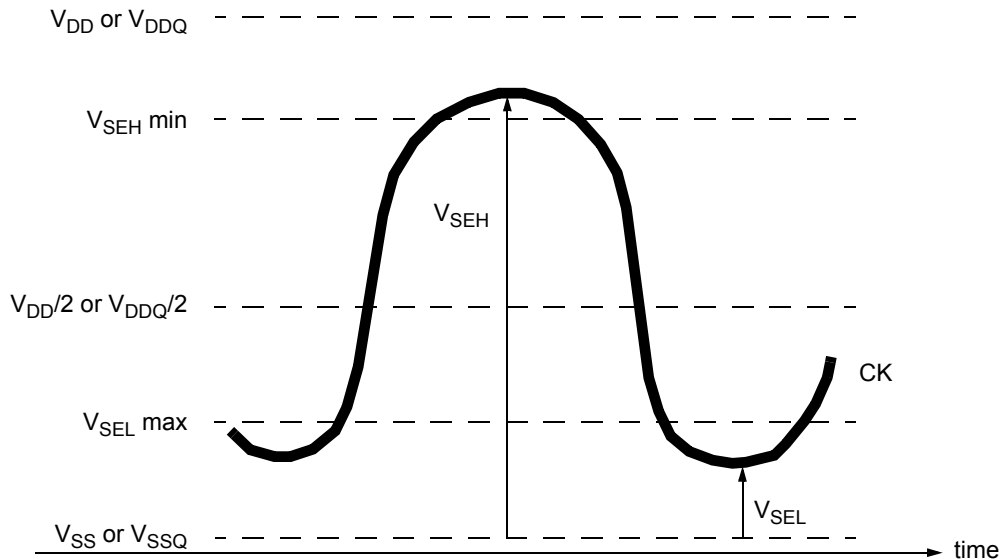


Figure 3. Single-ended requirement for differential signals.

Note that, while ADD/CMD signal requirements are with respect to V<sub>ref</sub>CA, the single-ended components of differential signals have a requirement with respect to V<sub>DD</sub> / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V<sub>SEL</sub>max, V<sub>SEH</sub>min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[ Table 7 ] Single-ended Levels for CK<sub>t</sub>, CK<sub>c</sub>

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		Unit	NOTE
		Min	Max	Min	Max		
V <sub>SEH</sub>	Single-ended high-level for CK <sub>t</sub> , CK <sub>c</sub>	(V <sub>DD</sub> /2)+0.100	NOTE3	TBD	NOTE3	V	1, 2
V <sub>SEL</sub>	Single-ended low-level for CK <sub>t</sub> , CK <sub>c</sub>	NOTE3	(V <sub>DD</sub> /2)-0.100	NOTE3	TBD	V	1, 2

**NOTE:**

1. For CK<sub>t</sub> - CK<sub>c</sub> use V<sub>IH</sub>.CA/V<sub>IL</sub>.CA(AC) of ADD/CMD;
2. V<sub>IH</sub>(AC)/V<sub>IL</sub>(AC) for ADD/CMD is based on V<sub>REF</sub>CA;
3. These values are not defined, however the single-ended signals CK<sub>t</sub> - CK<sub>c</sub> need to be within the respective limits (V<sub>IH</sub>.CA(DC) max, V<sub>IL</sub>.CA(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

## 12.4 Slew Rate Definitions

### 12.4.1 Slew Rate Definitions for Differential Input Signals (CK)

[ Table 8 ] Differential Input Slew Rate Definition

Description			Defined by
	from	to	
Differential input slew rate for rising edge(CK_t - CK_c)	V <sub>ILdiffmax</sub>	V <sub>IHdiffmin</sub>	[ V <sub>IHdiffmin</sub> - V <sub>ILdiffmax</sub> ] / DeltaTRdiff
Differential input slew rate for falling edge(CK_t - CK_c)	V <sub>IHdiffmin</sub>	V <sub>ILdiffmax</sub>	[ V <sub>IHdiffmin</sub> - V <sub>ILdiffmax</sub> ] / DeltaTFdiff
NOTE: The differential signal (i.e.,CK_t - CK_c) must be linear between these thresholds.			

**NOTE:** The differential signal (i.e., CK\_t - CK\_c) must be linear between these thresholds.

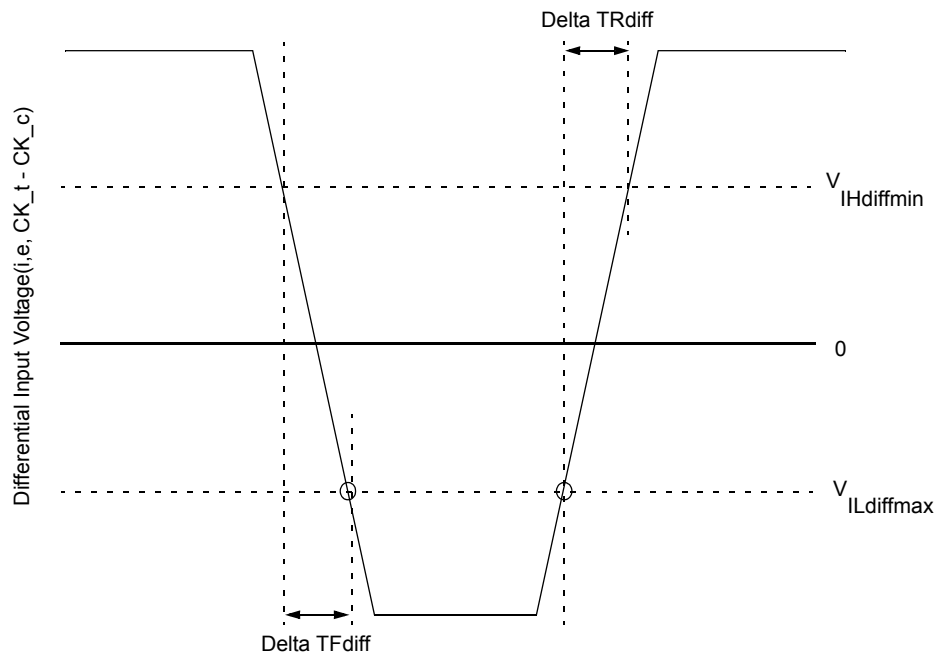


Figure 4. Differential Input Slew Rate Definition for CK\_t, CK\_c

## 12.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK\_t, CK\_c) must meet the requirements in Table 9. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

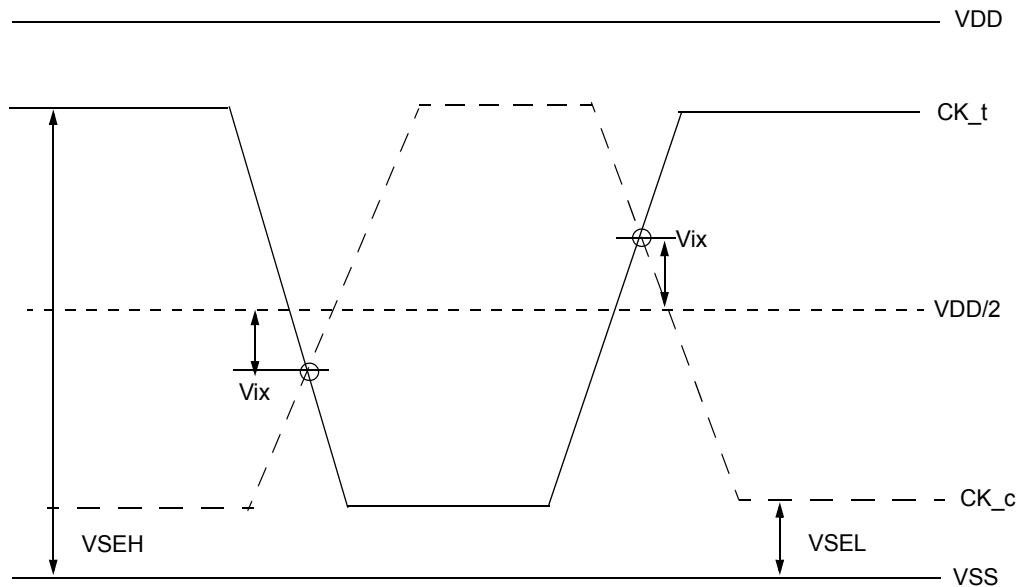


Figure 5. Vix Definition (CK)

[ Table 9 ] Cross Point Voltage for Differential Input Signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133			
		min		max	
-	Area of VSEH, VSEL	$VSEL \leq VDD/2 - 145mV$	$VDD/2 - 145mV \leq VSEL \leq VDD/2 - 100mV$	$VDD/2 + 100mV \leq VSEH \leq VDD/2 + 145mV$	$VDD/2 + 145mV \leq VSEH$
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-120mV	$-(VDD/2 - VSEL) + 25mV$	$(VSEH - VDD/2) - 25mV$	120mV

Symbol	Parameter	DDR4-2400/2666			
		min		max	
-	Area of VSEH, VSEL	TBD	TBD	TBD	TBD
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	TBD	TBD	TBD	TBD

## 12.6 Single-ended AC & DC Output Levels

[ Table 10 ] Single-ended AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666	Units	NOTE
$V_{OH}(DC)$	DC output high measurement level (for IV curve linearity)	$1.1 \times V_{DDQ}$	V	
$V_{OM}(DC)$	DC output mid measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OL}(DC)$	DC output low measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OH}(AC)$	AC output high measurement level (for output SR)	$(0.7 - 0.15) \times V_{DDQ}$	V	1
$V_{OL}(AC)$	AC output low measurement level (for output SR)	$(0.7 - 0.15) \times V_{DDQ}$	V	1

**NOTE:**

1. The swing of  $\pm 0.15 \times V_{DDQ}$  is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of  $R_{ZQ}/7\Omega$  and an effective test load of  $50\Omega$  to  $V_{TT} = V_{DDQ}$ .

## 12.7 Differential AC & DC Output Levels

[ Table 11 ] Differential AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666	Units	NOTE
$V_{OHdiff}(AC)$	AC differential output high measurement level (for output SR)	$+0.3 \times V_{DDQ}$	V	1
$V_{OLdiff}(AC)$	AC differential output low measurement level (for output SR)	$-0.3 \times V_{DDQ}$	V	1

**NOTE:**

1. The swing of  $\pm 0.3 \times V_{DDQ}$  is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of  $R_{ZQ}/7\Omega$  and an effective test load of  $50\Omega$  to  $V_{TT} = V_{DDQ}$  at each of the differential outputs.

## 12.8 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between  $V_{OL}(AC)$  and  $V_{OH}(AC)$  for single ended signals as shown in Table 12 and Figure 6.

[ Table 12 ] Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL}(AC)$	$V_{OH}(AC)$	$[V_{OH}(AC) - V_{OL}(AC)] / \Delta TRse$
Single ended output slew rate for falling edge	$V_{OH}(AC)$	$V_{OL}(AC)$	$[V_{OH}(AC) - V_{OL}(AC)] / \Delta TFse$

**NOTE:**

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

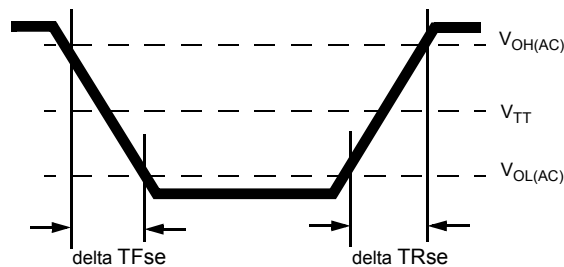


Figure 6. Single-ended Output Slew Rate Definition

## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

[ Table 13 ] Single-ended Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

**NOTE:**

1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.

-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

## 12.9 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 14 and Figure 7.

[ Table 14 ] Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)] / \Delta TR_{diff}$
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)] / \Delta TF_{diff}$

**NOTE:**

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

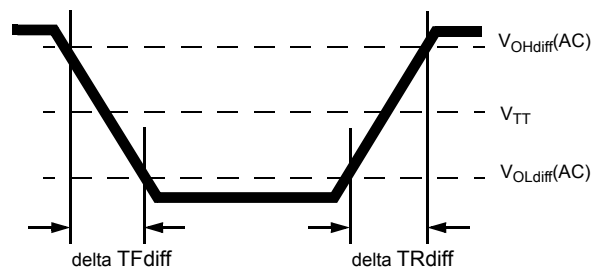


Figure 7. Differential Output Slew Rate Definition

[ Table 15 ] Differential Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	8	18	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

For Ron = RZQ/7 setting

## 12.10 Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

[ Table 16 ] Single-ended AC & DC Output Levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	$1.1 \times V_{DDQ}$	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	$0.2 \times V_{DDQ}$	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	$V_{TT} + (0.1 \times V_{DDQ})$	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	$V_{TT} - (0.1 \times V_{DDQ})$	V	1

**NOTE:**

1. The effective test load is  $50\Omega$  terminated by  $V_{TT} = 0.5 \times V_{DDQ}$ .

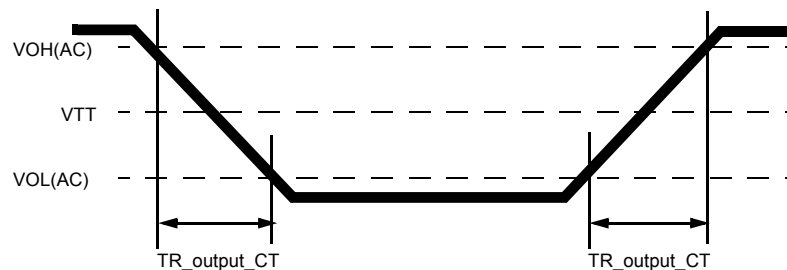


Figure 8. Output Slew Rate Definition of Connectivity Test Mode

[ Table 17 ] Single-ended Output Slew Rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133/2400/2666		Unit	Notes
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

## 12.11 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 9.

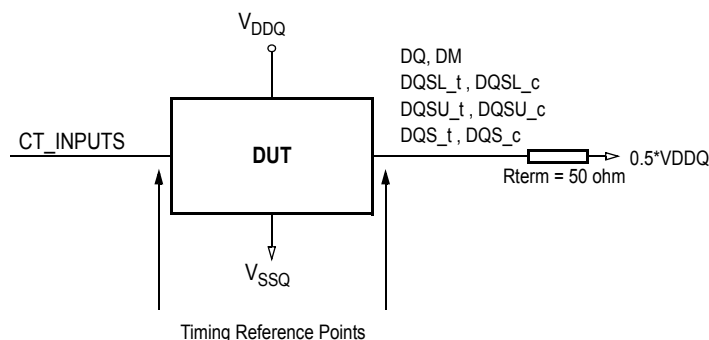


Figure 9. Connectivity Test Mode Timing Reference Load

## 13. DIMM IDD Specification Definition

[ Table 18 ] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	<b>Operating One Bank Active-Precharge Current (AL=0)</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, nRC, nRAS, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> High between ACT and PRE; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> Cycling with one bank active at a time: 0,0,1,1,2,2,...; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern
IDD0A	<b>Operating One Bank Active-Precharge Current (AL=CL-1)</b> <b>AL = CL-1, Other conditions:</b> see IDD0
IPP0	<b>Operating One Bank Active-Precharge IPP Current</b> <b>Same condition with IDD0</b>
IDD1	<b>Operating One Bank Active-Read-Precharge Current (AL=0)</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, nRC, nRAS, nRCD, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> High between ACT, RD and PRE; <b>Command, Address, Bank Group Address, Bank Address Inputs, Data IO:</b> partially toggling; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> Cycling with one bank active at a time: 0,0,1,1,2,2,...; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern
IDD1A	<b>Operating One Bank Active-Read-Precharge Current (AL=CL-1)</b> <b>AL = CL-1, Other conditions:</b> see IDD1
IPP1	<b>Operating One Bank Active-Read-Precharge IPP Current</b> <b>Same condition with IDD1</b>
IDD2N	<b>Precharge Standby Current (AL=0)</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern
IDD2NA	<b>Precharge Standby Current (AL=CL-1)</b> <b>AL = CL-1, Other conditions:</b> see IDD2N
IPP2N	<b>Precharge Standby IPP Current</b> <b>Same condition with IDD2N</b>
IDD2NT	<b>Precharge Standby ODT Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling; <b>Data IO:</b> VSSQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> toggling according; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern
IDDQ2NT (Optional)	<b>Precharge Standby ODT IDDQ Current</b> <b>Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current</b>
IDD2NL	<b>Precharge Standby Current with CAL enabled</b> <b>Same definition like for IDD2N, CAL enabled<sup>3</sup></b>
IDD2NG	<b>Precharge Standby Current with Gear Down mode enabled</b> <b>Same definition like for IDD2N, Gear Down mode enabled<sup>3,5</sup></b>
IDD2ND	<b>Precharge Standby Current with DLL disabled</b> <b>Same definition like for IDD2N, DLL disabled<sup>3</sup></b>
IDD2N_par	<b>Precharge Standby Current with CA parity enabled</b> <b>Same definition like for IDD2N, CA parity enabled<sup>3</sup></b>
IDD2P	<b>Precharge Power-Down Current</b> <b>CKE:</b> Low; <b>External clock:</b> On; <b>tCK, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0
IPP2P	<b>Precharge Power-Down IPP Current</b> <b>Same condition with IDD2P</b>
IDD2Q	<b>Precharge Quiet Standby Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0

## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

Symbol	Description
IDD3N	<b>Active Standby Current</b> CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 <sup>1</sup> ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD3NA	<b>Active Standby Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD3N
IPP3N	<b>Active Standby IPP Current</b> Same condition with IDD3N
IDD3P	<b>Active Power-Down Current</b> CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 <sup>1</sup> ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0
IPP3P	<b>Active Power-Down IPP Current</b> Same condition with IDD3P
IDD4R	<b>Operating Burst Read Current</b> CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 <sup>2</sup> ; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one according; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD4RA	<b>Operating Burst Read Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD4R
IDD4RB	<b>Operating Burst Read Current with Read DBI</b> Read DBI enabled <sup>3</sup> , Other conditions: see IDD4R
IPP4R	<b>Operating Burst Read IPP Current</b> Same condition with IDD4R
IDDQ4R (Optional)	<b>Operating Burst Read IDDQ Current</b> Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	<b>Operating Burst Read IDDQ Current with Read DBI</b> Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	<b>Operating Burst Write Current</b> CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 <sup>1</sup> ; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern
IDD4WA	<b>Operating Burst Write Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD4W
IDD4WB	<b>Operating Burst Write Current with Write DBI</b> Write DBI enabled <sup>3</sup> , Other conditions: see IDD4W
IDD4WC	<b>Operating Burst Write Current with Write CRC</b> Write CRC enabled <sup>3</sup> , Other conditions: see IDD4W
IDD4W_par	<b>Operating Burst Write Current with CA Parity</b> CA Parity enabled <sup>3</sup> , Other conditions: see IDD4W
IPP4W	<b>Operating Burst Write IPP Current</b> Same condition with IDD4W
IDD5B	<b>Burst Refresh Current (1X REF)</b> CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 8 <sup>1</sup> ; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IPP5B	<b>Burst Refresh Write IPP Current (1X REF)</b> Same condition with IDD5B
IDD5F2	<b>Burst Refresh Current (2X REF)</b> tRFC=tRFC_x2, Other conditions: see IDD5B
IPP5F2	<b>Burst Refresh Write IPP Current (2X REF)</b> Same condition with IDD5F2



## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

Symbol	Description
IDD5F4	<b>Burst Refresh Current (4X REF)</b> <b>tRFC=tRFC_x4, Other conditions:</b> see IDD5B
IPP5F4	<b>Burst Refresh Write IPP Current (4X REF)</b> <b>Same condition with IDD5F4</b>
IDD6N	<b>Self Refresh Current: Normal Temperature Range</b> <b>T<sub>CASE</sub>:</b> 0 - 85°C; <b>Low Power Array Self Refresh (LP ASR):</b> Normal <sup>4</sup> ; <b>CKE:</b> Low; <b>External clock:</b> Off; <b>CK<sub>t</sub></b> and <b>CK<sub>c</sub></b> : LOW; <b>CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS<sub>n</sub></b> , <b>Command, Address, Bank Group Address, Bank Address, Data IO:</b> High; <b>DM<sub>n</sub>:</b> stable at 1; <b>Bank Activity:</b> Self-Refresh operation; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> MID-LEVEL
IPP6N	<b>Self Refresh IPP Current: Normal Temperature Range</b> <b>Same condition with IDD6N</b>
IDD6E	<b>Self-Refresh Current: Extended Temperature Range</b> <b>T<sub>CASE</sub>:</b> 0 - 95°C; <b>Low Power Array Self Refresh (LP ASR):</b> Extended <sup>4</sup> ; <b>CKE:</b> Low; <b>External clock:</b> Off; <b>CK<sub>t</sub></b> and <b>CK<sub>c</sub></b> : LOW; <b>CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS<sub>n</sub></b> , <b>Command, Address, Bank Group Address, Bank Address, Data IO:</b> High; <b>DM<sub>n</sub>:</b> stable at 1; <b>Bank Activity:</b> Extended Temperature Self-Refresh operation; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> MID-LEVEL
IPP6E	<b>Self Refresh IPP Current: Extended Temperature Range</b> <b>Same condition with IDD6E</b>
IDD6R	<b>Self-Refresh Current: Reduced Temperature Range</b> <b>T<sub>CASE</sub>:</b> 0 - 45°C; <b>Low Power Array Self Refresh (LP ASR):</b> Reduced <sup>4</sup> ; <b>CKE:</b> Low; <b>External clock:</b> Off; <b>CK<sub>t</sub></b> and <b>CK<sub>c</sub></b> : LOW; <b>CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS<sub>n</sub></b> , <b>Command, Address, Bank Group Address, Bank Address, Data IO:</b> High; <b>DM<sub>n</sub>:</b> stable at 1; <b>Bank Activity:</b> Extended Temperature Self-Refresh operation; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> MID-LEVEL
IPP6R	<b>Self Refresh IPP Current: Reduced Temperature Range</b> <b>Same condition with IDD6R</b>
IDD6A	<b>Auto Self-Refresh Current</b> <b>T<sub>CASE</sub>:</b> 0 - 95°C; <b>Low Power Array Self Refresh (LP ASR):</b> Auto <sup>4</sup> ; <b>CKE:</b> Low; <b>External clock:</b> Off; <b>CK<sub>t</sub></b> and <b>CK<sub>c</sub></b> : LOW; <b>CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS<sub>n</sub></b> , <b>Command, Address, Bank Group Address, Bank Address, Data IO:</b> High; <b>DM<sub>n</sub>:</b> stable at 1; <b>Bank Activity:</b> Auto Self-Refresh operation; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> MID-LEVEL
IPP6A	<b>Auto Self-Refresh IPP Current</b> <b>Same condition with IDD6A</b>
IDD7	<b>Operating Bank Interleave Read Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> CL-1; <b>CS<sub>n</sub>:</b> High between ACT and RDA; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling; <b>Data IO:</b> read data bursts with different data between one burst and the next one; <b>DM<sub>n</sub>:</b> stable at 1; <b>Bank Activity:</b> two times interleaved cycling through banks (0, 1, ...7) with different addressing; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern
IPP7	<b>Operating Bank Interleave Read IPP Current</b> <b>Same condition with IDD7</b>
IDD8	<b>Maximum Power Down Current TBD</b>
IPP8	<b>Maximum Power Down IPP Current Same condition with IDD8</b>

## NOTE:

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].

2. Output Buffer Enable

- set MR1 [A12 = 0]: Qoff = Output buffer enabled

- set MR1 [A2:1 = 00]: Output Driver Impedance Control = RZQ/7

RTT\_Nom enable

- set MR1 [A10:8 = 011]: RTT\_NOM = RZQ/6

RTT\_WR enable

- set MR2 [A10:9 = 01]: RTT\_WR = RZQ/2

RTT\_PARK disable

- set MR5 [A8:6 = 000]

3. CAL enabled: set MR4 [A8:6 = 001]: 1600MT/s

010]: 1866MT/s, 2133MT/s

011]: 2400MT/s, 2666MT/s

Gear Down mode enabled: set MR3 [A3 = 1]: 1/4 Rate

DLL disabled: set MR1 [A0 = 0]

CA parity enabled: set MR5 [A2:0 = 001]: 1600MT/s, 1866MT/s, 2133MT/s

010]: 2400MT/s, 2666MT/s

Read DBI enabled: set MR5 [A12 = 1]

Write DBI enabled: set MR5 [A11 = 1]

4. Low Power Array Self Refresh (LP ASR): set MR2 [A7:6 = 00]: Normal

01]: Reduced Temperature range

10]: Extended Temperature range

11]: Auto Self Refresh

5. IDD2NG should be measured after sync pules (NOP) input.

## 14. IDD SPEC Table

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

[ Table 19 ]  $I_{DD}$  and  $I_{DDQ}$  Specification

Symbol	M386A8K40BM1 : 64GB(8Gx72) Module				M386A8K40BM2 : 64GB(8Gx72) Module		Unit	NOTE
	DDR4-2133		DDR4-2400		DDR4-2666			
	15-15-15		17-17-17		19-19-19			
	VDD 1.2V	VPP2.5V	VDD 1.2V	VPP2.5V	VDD 1.2V	VPP2.5V		
	IDD Max.	IPP Max.	IDD Max.	IPP Max.	IDD Max.	IPP Max.		
$I_{DD0}$	2674	234	2848	234	2982	234	mA	
$I_{DD0A}$	2698	234	2895	234	3046	234	mA	
$I_{DD1}$	3230	234	3427	234	3586	234	mA	
$I_{DD1A}$	3267	234	3473	234	3647	234	mA	
$I_{DD2N}$	2549	216	2727	216	2847	216	mA	
$I_{DD2NA}$	2664	216	2873	216	3034	216	mA	
$I_{DD2NT}$	2603	216	2820	216	2949	216	mA	
$I_{DD2NL}$	2129	216	2274	216	2372	216	mA	
$I_{DD2NG}$	2483	216	2662	216	2773	216	mA	
$I_{DD2ND}$	2369	216	2535	216	2636	216	mA	
$I_{DD2N\_par}$	2613	216	2788	216	2903	216	mA	
$I_{DD2P}$	1493	216	1601	216	1655	216	mA	
$I_{DD2Q}$	2375	216	2539	216	2641	216	mA	
$I_{DD3N}$	3088	216	3355	216	3502	216	mA	
$I_{DD3NA}$	3241	216	3530	216	3716	216	mA	
$I_{DD3P}$	1791	216	1976	216	2045	216	mA	
$I_{DD4R}$	4485	216	4814	216	5124	216	mA	
$I_{DD4RA}$	4544	216	4882	216	5208	216	mA	
$I_{DD4RB}$	4507	216	4839	216	5155	216	mA	
$I_{DD4W}$	4498	216	4833	216	5147	216	mA	
$I_{DD4WA}$	4563	216	4904	216	5226	216	mA	
$I_{DD4WB}$	4498	216	4833	216	5145	216	mA	
$I_{DD4WC}$	4456	216	4726	216	5019	216	mA	
$I_{DD4W\_par}$	4643	216	5005	216	5317	216	mA	
$I_{DD5B}$	5556	486	5758	486	5827	486	mA	
$I_{DD5F2}$	4600	432	4794	432	4866	432	mA	
$I_{DD5F4}$	4231	414	4421	414	4465	414	mA	
$I_{DD6N}$	1345	288	1469	288	1472	288	mA	
$I_{DD6E}$	2094	360	2233	360	2236	360	mA	
$I_{DD6R}$	978	252	1083	252	1087	252	mA	
$I_{DD6A}$	1305	288	1404	288	1408	288	mA	
$I_{DD7}$	5924	306	6423	315	6931	315	mA	
$I_{DD8}$	567	216	653	216	657	216	mA	

### NOTE :

1. DIMM IDD SPEC is based on the condition that de-activated rank(IDLE) is IDD2N. Please refer to Table20.
2. IDD current measure method and detail patterns are described on DDR4 component datasheet.
3. VDD and VDDQ are merged on module PCB ( IDDQ values are not considered by Qoff condition)
4. DIMM IDD Values are calculated based on the component IDD spec and Register power.

## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

[ Table 20 ] DIMM Rank Status

SEC DIMM	Operating Rank	The other Rank
<i>I</i> <sub>DD0</sub>	<i>I</i> <sub>DD0</sub>	<i>I</i> <sub>DD2N</sub>
<i>I</i> <sub>DD1</sub>	<i>I</i> <sub>DD1</sub>	<i>I</i> <sub>DD2N</sub>
<i>I</i> <sub>DD2P</sub>	<i>I</i> <sub>DD2P</sub>	<i>I</i> <sub>DD2P</sub>
<i>I</i> <sub>DD2N</sub>	<i>I</i> <sub>DD2N</sub>	<i>I</i> <sub>DD2N</sub>
<i>I</i> <sub>DD2Q</sub>	<i>I</i> <sub>DD2Q</sub>	<i>I</i> <sub>DD2Q</sub>
<i>I</i> <sub>DD3P</sub>	<i>I</i> <sub>DD3P</sub>	<i>I</i> <sub>DD3P</sub>
<i>I</i> <sub>DD3N</sub>	<i>I</i> <sub>DD3N</sub>	<i>I</i> <sub>DD3N</sub>
<i>I</i> <sub>DD4R</sub>	<i>I</i> <sub>DD4R</sub>	<i>I</i> <sub>DD2N</sub>
<i>I</i> <sub>DD4W</sub>	<i>I</i> <sub>DD4W</sub>	<i>I</i> <sub>DD2N</sub>
<i>I</i> <sub>DD5B</sub>	<i>I</i> <sub>DD5B</sub>	<i>I</i> <sub>DD2N</sub>
<i>I</i> <sub>DD6</sub>	<i>I</i> <sub>DD6</sub>	<i>I</i> <sub>DD6</sub>
<i>I</i> <sub>DD7</sub>	<i>I</i> <sub>DD7</sub>	<i>I</i> <sub>DD2N</sub>
<i>I</i> <sub>DD8</sub>	<i>I</i> <sub>DD8</sub>	<i>I</i> <sub>DD8</sub>

## 15. Input/Output Capacitance

[ Table 21 ] Silicon Pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		Unit	NOTE
		min	max	min	max		
C <sub>IO</sub>	Input/output capacitance	0.55	1.4	0.55	1.15	pF	1,2,3
C <sub>DIO</sub>	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C <sub>DDQS</sub>	Input/output capacitance delta DQS <sub>t</sub> and DQS <sub>c</sub>	-	0.05	-	0.05	pF	1,2,3,5
C <sub>CK</sub>	Input capacitance, CK <sub>t</sub> and CK <sub>c</sub>	0.2	0.8	0.2	0.7	pF	1,3
C <sub>DCK</sub>	Input capacitance delta CK <sub>t</sub> and CK <sub>c</sub>	-	0.05	-	0.05	pF	1,3,4
C <sub>I</sub>	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	pF	1,3,6
C <sub>DI_CTRL</sub>	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
C <sub>DI_ADD_CMD</sub>	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C <sub>ALERT</sub>	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	pF	1,3
C <sub>ZQ</sub>	Input/output capacitance of ZQ	-	2.3	-	2.3	pF	1,3,12
C <sub>TEN</sub>	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,3,13

### NOTE:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.
2. DQ, DM<sub>n</sub>, DQS<sub>T</sub>, DQS<sub>c</sub>, TDQS<sub>T</sub>, TDQS<sub>C</sub>. Although the DM, TDQS<sub>T</sub> and TDQS<sub>C</sub> pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK<sub>T</sub>-CK<sub>C</sub>
5. Absolute value of CIO(DQS<sub>T</sub>)-CIO (DQS<sub>c</sub>)
6. CI applies to ODT, CS<sub>n</sub>, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS<sub>n</sub>/A16, CAS<sub>n</sub>/A15, WE<sub>n</sub>/A14, ACT<sub>n</sub> and PAR.
7. CDI\_CTRL applies to ODT, CS<sub>n</sub> and CKE
8. CDI\_CTRL = CI(CTRL)-0.5\*(CI(CLK<sub>T</sub>)+CI(CLK<sub>C</sub>))
9. CDI\_ADD\_CMD applies to, A0-A17, BA0-BA1, BG0-BG1, RAS<sub>n</sub>/A16, CAS<sub>n</sub>/A15, WE<sub>n</sub>/A14, ACT<sub>n</sub> and PAR.
10. CDI\_ADD\_CMD = CI(ADD\_CMD)-0.5\*(CI(CLK<sub>T</sub>)+CI(CLK<sub>C</sub>))
11. CDIO = CIO(DQ,DM)-0.5\*(CIO(DQS<sub>T</sub>)+CIO(DQS<sub>c</sub>))
12. Maximum external load capacitance on ZQ pin: tbd pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

Load Reduced DIMM

datasheet

DDR4 SDRAM

## 16. Electrical Characteristics and AC Timing

### 16.1 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

[ Table 22 ] DDR4-1600 Speed Bins and Operations

Speed Bin			DDR4-1600		Unit	NOTE	
CL-nRCD-nRP			11-11-11				
Parameter		Symbol	min	max			
Internal read command to first data		tAA	13.75 <sup>13</sup> (13.50) <sup>5,11</sup>	18.00	ns	11	
Internal read command to first data with read DBI enabled		tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	11	
ACT to internal read or write delay time		tRCD	13.75 <sup>13</sup> (13.50) <sup>5,11</sup>	-	ns	11	
PRE command period		tRP	13.75 <sup>13</sup> (13.50) <sup>5,11</sup>	-	ns	11	
ACT to PRE command period		tRAS	35	9 x tREFI	ns	11	
ACT to ACT or REF command period		tRC	48.75 (48.50) <sup>5,11</sup>	-	ns	11	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional) <sup>5,11</sup>	1.6	ns	1,2,3,4,10,13
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings			9,11,12		nCK	12,13	
Supported CL Settings with read DBI			11,13,14		nCK	12	
Supported CWL Settings			9,11		nCK		

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## datasheet

## DDR4 SDRAM

[ Table 23 ] DDR4-1866 Speed Bins and Operations

Speed Bin			DDR4-1866		Unit	NOTE	
CL-nRCD-nRP			13-13-13				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		13.92 <sup>13</sup> (13.50) <sup>5,11</sup>	18.00	ns	11	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 2nCK	tAA(max) + 2nCK	ns	11	
ACT to internal read or write delay time	tRCD		13.92 <sup>13</sup> (13.50) <sup>5,11</sup>	-	ns	11	
PRE command period	tRP		13.92 <sup>13</sup> (13.50) <sup>5,11</sup>	-	ns	11	
ACT to PRE command period	tRAS		34	9 x tREFI	ns	11	
ACT to ACT or REF command period	tRC		47.92 (47.50) <sup>5,11</sup>	-	ns	11	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional) <sup>5,11</sup>	1.6	ns	1,2,3,4,10,13
	CL = 10	CL = 12	tCK(AVG)	Reserved			
	CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns
CL = 11		CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
				(Optional) <sup>5,11</sup>			
CL = 12		CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings			9,11,12,13,14		nCK	12,13	
Supported CL Settings with read DBI			11,13,14,15,16		nCK	12	
Supported CWL Settings			9,10,11,12		nCK		

## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

[ Table 24 ] DDR4-2133 Speed Bins and Operations

Speed Bin			DDR4-2133		Unit	NOTE	
CL-nRCD-nRP			15-15-15				
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.06 <sup>13</sup> (13.75) <sup>5,11</sup>	18.00	ns	11
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11
ACT to internal read or write delay time			tRCD	14.06 (13.75) <sup>5,11</sup>	-	ns	11
PRE command period			tRP	14.06 (13.75) <sup>5,11</sup>	-	ns	11
ACT to PRE command period			tRAS	33	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	47.06 (46.75) <sup>5,11</sup>	-	ns	11
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional) <sup>5,11</sup>	1.6	ns	1,2,3,4,10,13
	CL = 10	CL = 12	tCK(AVG)	Reserved			
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional) <sup>5,11</sup>	<1.5	ns	1,2,3,4,7
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5		
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071 (Optional) <sup>5,11</sup>	<1.25	ns	1,2,3,4,7
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25		
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3
Supported CL Settings			9,11,12,13,14,15,16			nCK	12,13
Supported CL Settings with read DBI			11,13,14,15,16,18,19			nCK	
Supported CWL Settings			9,10,11,12,14			nCK	

## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

[ Table 25 ] DDR4-2400 Speed Bins and Operations

Speed Bin			DDR4-2400		Unit	NOTE	
CL-nRCD-nRP			17-17-17				
Parameter		Symbol	min	max			
Internal read command to first data		tAA	14.16 (13.75) <sup>5,11</sup>	18.00	ns	11	
Internal read command to first data with read DBI enabled		tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11	
ACT to internal read or write delay time		tRCD	14.16 (13.75) <sup>5,11</sup>	-	ns	11	
PRE command period		tRP	14.16 (13.75) <sup>5,11</sup>	-	ns	11	
ACT to PRE command period		tRAS	32	9 x tREFI	ns	11	
ACT to ACT or REF command period		tRC	46.16 (45.75) <sup>5,11</sup>	-	ns	11	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
				(Optional) <sup>5,11</sup>			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
				(Optional) <sup>5,11</sup>			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8
				(Optional) <sup>5,11</sup>			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937		
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings			10,11,12,13,14,15,16,17,18		nCK	12,13	
Supported CL Settings with read DBI			12,13,14,15,16,18,19,20,21		nCK		
Supported CWL Settings			9,10,11,12,14,16		nCK		



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## datasheet

## DDR4 SDRAM

[ Table 26 ] DDR4-2666 Speed Bins and Operations

Speed Bin			DDR4-2666		Unit	NOTE	
CL-nRCD-nRP			19-19-19				
Parameter		Symbol	min	max			
Internal read command to first data		tAA	14.25 <sup>14</sup> (13.75) <sup>5,12</sup>	18.00	ns	11	
Internal read command to first data with read DBI enabled		tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11	
ACT to internal read or write delay time		tRCD	14.25 (13.75) <sup>5,12</sup>	-	ns	11	
PRE command period		tRP	14.25 <sup>14</sup> (13.75) <sup>5,12</sup>	-	ns	11	
ACT to PRE command period		tRAS	32	9 x tREFI	ns	11	
ACT to ACT or REF command period		tRC	46.25 (45.75) <sup>5,12</sup>	-	ns	11	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
				(Optional) <sup>5,12</sup>			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
				(Optional) <sup>5,12</sup>			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
				(Optional) <sup>5,12</sup>			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
				(Optional) <sup>5,12</sup>			1,2,3,4,9
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings			10,11,12,13,14,15,16,17,18,19,20		nCK	12	
Supported CL Settings with read DBI			12,13,14,15,17,18,19,20,21,22,23		nCK		
Supported CWL Settings			9,10,11,12,14,16,18		nCK		

## 16.2 Speed Bin Table Note

### Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133, 2400 and 2666 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section 13.5.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071ns or 0.937ns or 0.833ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
11. Parameters apply from tCK(avg) min to tCK(avg) max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
12. CL number in parentheses, it means that these numbers are optional.
13. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
14. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

Load Reduced DIMM

datasheet

DDR4 SDRAM

# 17. Timing Parameters by Speed Grade

[ Table 27 ] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2666

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing													
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	0.750	<0.833	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot tCK(avg)m ax + tJIT(per)max_tot										tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	-38	38	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	-19	19	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	-30	30	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	125	-	107	-	94	-	83	-	75	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	100	-	86	-	75	-	67	-	60	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	-55	55	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	-66	66	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	-73	73	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	-78	78	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	-83	83	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	-87	87	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	-91	91	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	-94	94	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	-96	96	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	-99	99	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	-101	101	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	-103	103	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	-104	104	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	-106	106	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	-120	120	-108	108	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	-110	110	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	-112	112	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)										ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	TBD	-	ps	
Command and Address setup time to CK_t,CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	TBD	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	TBD	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	TBD	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	385	-	ps	
Command and Address Timing													
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5.625 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nC K,6ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nC K,5ns)	-	Max(4nC K,4.2ns)	-	Max(4nC K,3.7ns)	-	Max(4nC K,3.3ns)	-	Max(4nC K,3ns)	-	nCK	34

## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nC K, 5ns)		Max(4nC K, 4.2ns)		Max(4nC K, 3.7ns)		Max(4nC K, 3.3ns)	-	Max(4nC K, 3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nC K, 7.5ns)		Max(4nC K, 6.4ns)		Max(4nC K, 6.4ns)		Max(4nC K, 6.4ns)	-	Max(4nC K, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nC K, 6ns)		Max(4nC K, 5.3ns)		Max(4nC K, 5.3ns)		Max(4nC K, 4.9ns)	-	Max(4nC K, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nC K, 6ns)		Max(4nC K, 5.3ns)		Max(4nC K, 5.3ns)		Max(4nC K, 4.9ns)	-	Max(4nC K, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nC K, 35ns)		Max(28nC K, 30ns)		Max(28nC K, 30ns)		Max(28nC K, 30ns)	-	Max(28nC K, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nC K, 25ns)		Max(20nC K, 23ns)		Max(20nC K, 21ns)		Max(20nC K, 21ns)	-	Max(20nC K, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nC K, 20ns)		Max(16nC K, 17ns)		Max(16nC K, 15ns)		Max(16nC K, 13ns)	-	Max(16nC K, 13ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nC K, 2.5ns)	-	max(2nC K, 2.5ns)	-	max(2nC K, 2.5ns)	-	max(2nC K, 2.5ns)	-	max(2nC K, 2.5ns)	-	ns	1,2,e,3 4
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nC K, 7.5ns)	-	max(4nC K, 7.5ns)	-	max(4nC K, 7.5ns)	-	max(4nC K, 7.5 ns)	-	max(4nC K, 7.5 ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nC K, 7.5ns)	-	max(4nC K, 7.5ns)	-	max(4nC K, 7.5ns)	-	max(4nC K, 7.5 ns)	-	max(4nC K, 7.5 ns)	-		34
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max(4nC K, 3.7 5ns)	-	tWR+max(5nC K, 3.7 5ns)	-	tWR+max(5nC K, 3.7 5ns)	-	tWR+max(5nC K, 3.7 5ns)	-	tWR+max(5nC K, 3.7 5ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+ max(4nC K, 3.7 5ns)	-	tWTR_S+ max(5nC K, 3.7 5ns)	-	tWTR_S+ max(5nC K, 3.7 5ns)	-	tWTR_S+ max(5nC K, 3.7 5ns)	-	tWTR_S+ max(5nC K, 3.7 5ns)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+ max(4nC K, 3.7 5ns)	-	tWTR_L+ max(5nC K, 3.7 5ns)	-	tWTR_L+ max(5nC K, 3.7 5ns)	-	tWTR_L+ max(5nC K, 3.7 5ns)	-	tWTR_L+ max(5nC K, 3.7 5ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	854	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nC K, 15ns)	-	max(24nC K, 15ns)	-	max(24nC K, 15ns)	-	max(24nC K, 15ns)	-	max(24nC K, 15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))										nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47
<b>CS_n to Command Address Latency</b>													
CS_n to Command Address Latency	tCAL	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
<b>DRAM Data Timing</b>													
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.17	-	0.18	tCK(avg)/2	13,18,3 9,49
DQ output hold time per group, per access from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	0.74	-	tCK(avg)/2	13,17,1 8,39,49
Data Valid Window per device per UI: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	TBD	-	UI	17,18,3 9,49
Data Valid Window, per pin per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	0.72	-	UI	17,18,3 9,49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-390	180	-330	175	-310	170	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	225	-	195	-	180	-	175	-	170	ps	39
<b>Data Strobe Timing</b>													
DQS_t, DQS_c differential READ Pre-amble (1 clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	0.9	NOTE 44	0.9	NOTE 44	tCK	39,40

## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	1.8	NOTE 44	1.8	NOTE 44	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	39
DQS_t, DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t, DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	tWPRE2	NA	NA	NA	NA	NA	NA	1.8	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-330	175	-310	170	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	175	-	170	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSK (DLL On)	-225	225	-195	195	-180	180	-175	175	-170	170	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSKI (DLL On)		370		330		310		290		270	ps	37,38,39
<b>MPSM Timing</b>													
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	TBD	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	TBD	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	TBD	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	TBD	-		
CS setup time to CKE	tMPX_S	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	TBD	-		
<b>Calibration Timing</b>													
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	128	-	nCK	
<b>Reset/Self Refresh Timing</b>													
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK, tRFC(min)+10ns)	-	max (5nCK, tRFC(min)+10ns)	-	max (5nCK, tRFC(min)+10ns)	-	max (5nCK, tRFC(min)+10ns)	-	max (5nCK, tRFC(min)+10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and Gear Down)	tXS_FAST(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK	

## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max(5nCK, 10ns)+PL	-	max(5nCK, 10ns)+PL	-	max(5nCK, 10ns)+PL	-	max(5nCK, 10ns)+PL	-	max(5nCK, 10ns)+PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	nCK	
Power Down Timing													
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	nCK	
CKE minimum pulse width	tCKE	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+W R+1	-	WL+4+W R+1	-	WL+4+W R+1	-	WL+4+W R+1	-	WL+4+W R+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+W R+1	-	WL+2+W R+1	-	WL+2+W R+1	-	WL+2+W R+1	-	WL+2+W R+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	nCK	
PDA Timing													
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		tMOD		nCK	
ODT Timing													
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing													
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	0	2	ns	
CA Parity Timing													
Commands not guaranteed to be executed during this time	tPAR_UN-KNOWN	-	PL	-	PL	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	

## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Pulse width of ALERT_n signal when as-asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	80	160	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64		71	nCK	
Parity Latency	PL	4		4		4		5		5		nCK	
CRC Error Reporting													
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	6	10	nCK	
Geardown timing													
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	-	-	-	-	-	-	-	-	TBD			
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	-	-	-	-	-	-	-	-	TBD			
MRS command to Sync pulse time(T3)	tSYNC_GEAR	-	-	-	-	-	-	-	-	TBD	-		27
Sync pulse to First valid command(T4)	tCMD_GEAR	-	-	-	-	-	-	-	-	TBD			27
Geardown setup time	tGEAR_setup	-	-	-	-	-	-	-	-	2	-	nCK	
Geardown hold time	tGEAR_hold	-	-	-	-	-	-	-	-	2	-	nCK	
tREFI													
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	260	-	260	-	ns	34



## Load Reduced DIMM

## datasheet

## DDR4 SDRAM

## NOTE :

1. Start of internal write transaction is defined as follows :  
For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.  
For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.  
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK following rounding algorithm defined in "13.5 Rounding Algorithms".
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports  $t_{nPARAM}[nCK] = RU\{t_{PARAM}[ns]/t_{CK}(avg)[ns]\}$ , which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR\_CRC\_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR\_S\_CRC\_DM is used in place of tWTR\_S.
11. When CRC and DM are both enabled tWTR\_L\_CRC\_DM is used in place of tWTR\_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual  $t_{jit(per)}_{total}$  of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS\_t - DQS\_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS\_t - DQS\_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR\_CRC\_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR\_S\_CRC\_DM is used in place of tWTR\_S.
30. When CRC and DM are both enabled tWTR\_L\_CRC\_DM is used in place of tWTR\_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from  $t_{CK}(avg)_{min}$  to  $t_{CK}(avg)_{max}$  at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables shown in section 10.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.  
 $UI = t_{CK}(avg).min/2$
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM
39. Value is only valid for RZQ/7 RONNOM = 34 ohms
40. 1tCK toggle mode with setting MR4:A11 to 0
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666 speed grade.
42. 1tCK mode with setting MR4:A12 to 0
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. Relationship". Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47. VrefDQ value must be set to either its midpoint or Vcent\_DQ(midpoint) in order to capture DQ0 or DQ0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately  $0.7 * VDDQ$  as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to  $V_{TT} = VDDQ$ .
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.



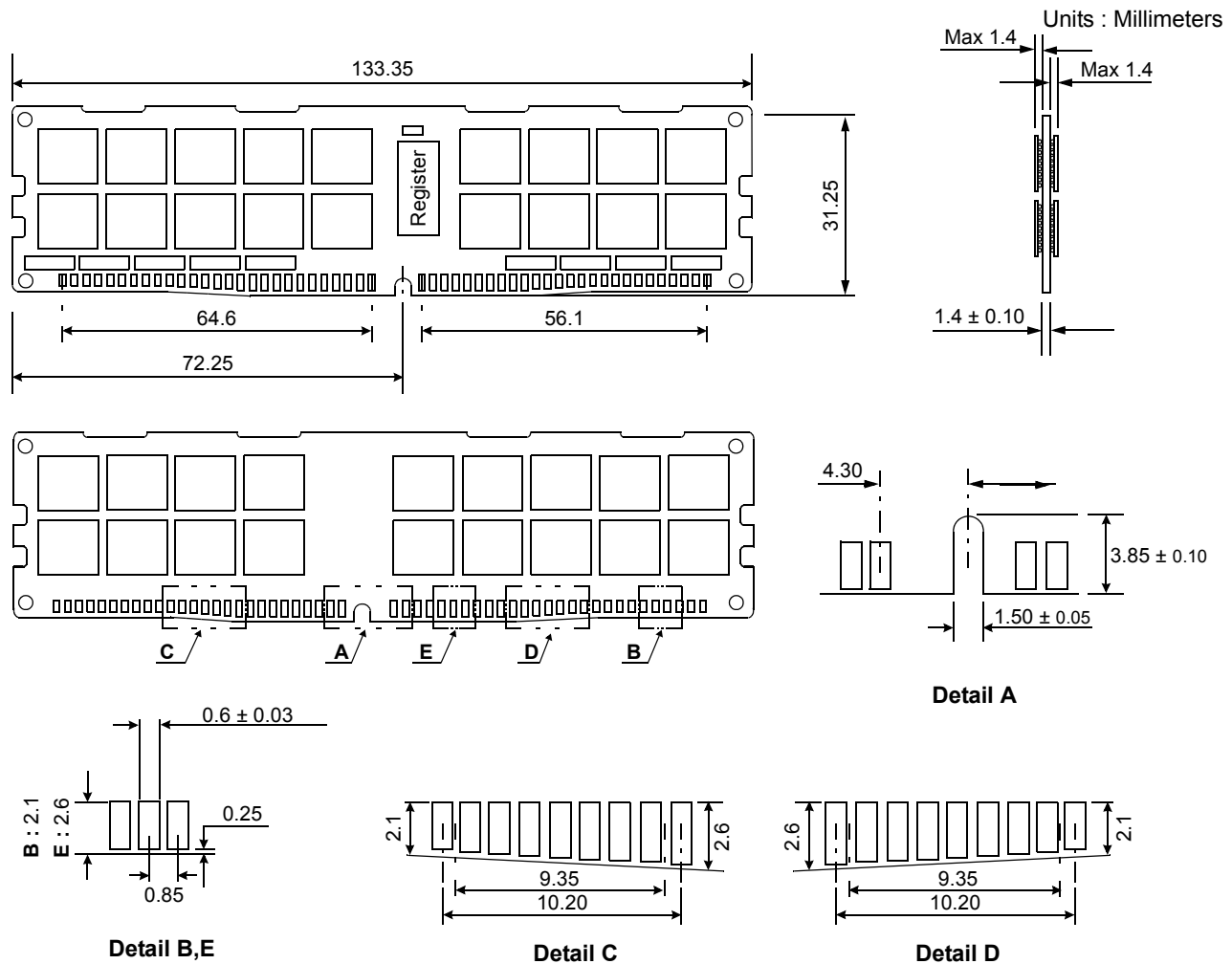
Load Reduced DIMM

datasheet

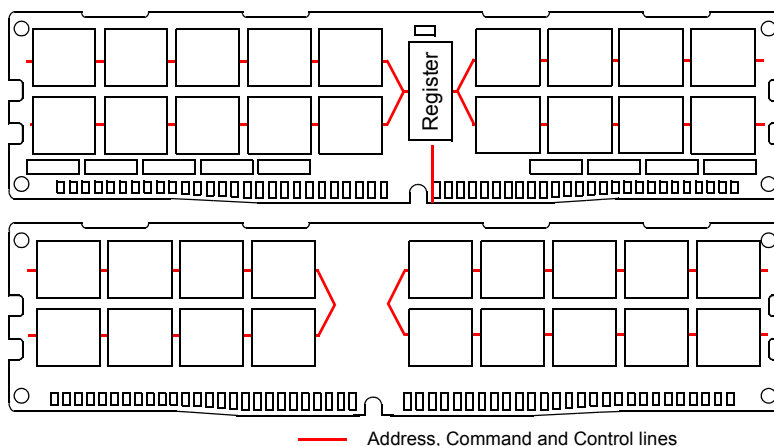
DDR4 SDRAM

## 18. Physical Dimensions

### 18.1 4Gbx4(DDP) based 8Gx72 Module (4 Ranks) - M386A8K40BM1/M386A8K40BM2



#### 18.1.1 x72 DIMM, populated as Quad physical ranks of x4 DDR4 SDRAMs

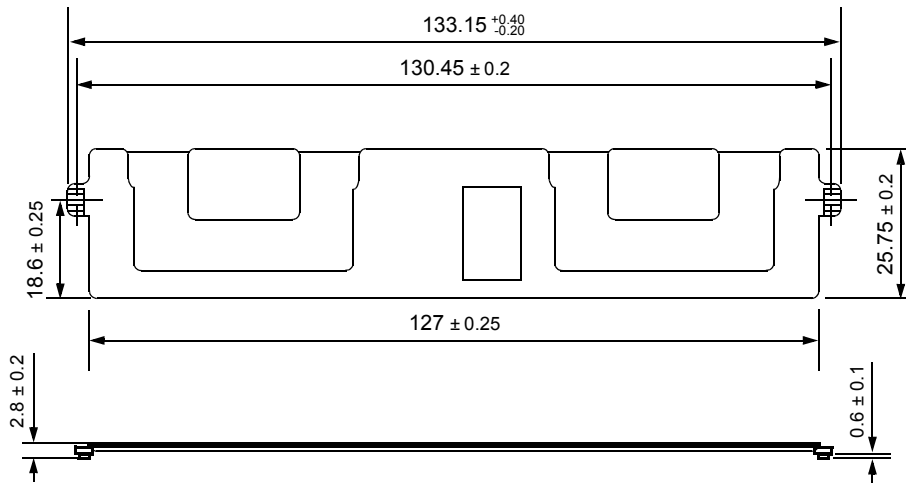


The used device is 4G x4(DDP) DDR4 SDRAM, FBGA.  
DDR4 SDRAM Part NO: K4AAG045WB-MC\*\*

\* **NOTE** : Tolerances on all dimensions ±0.15 unless otherwise specified.

## 18.1.2 Heat Spreader Design Guide

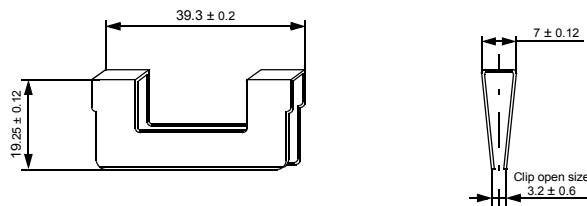
### 1. FRONT PART



### 2. BACK PART



### 3. CLIP PART



### 4. DDR4 RDIMM ASS'Y View

Reference thickness total (Maximum) : 7.30 (With Clip thickness)

H/S Assy



H/S, Clip Assy

